WHAT IS CLAIMED IS:

1. A circuit comprising:

a buffer for storing data, wherein the buffer includes a plurality of entries;

a write pointer coupled to the buffer, wherein the write pointer is configured to sequentially indicate each one of the plurality of entries in the buffer into which data is to be written, wherein the write pointer is clocked by a first clock;

a read pointer coupled to the buffer, wherein the read pointer is configured to sequentially indicate each one of said plurality of entries in the buffer from which data is to be read, wherein the read pointer is clocked by a second clock; and

a first circuit configured to generate a pointer value in response to an indication that a predetermined pattern of data is transmitted to the buffer for storage, wherein the first circuit is coupled to the read pointer;

a synchronizing circuit coupled to the read pointer and to receive the indication, wherein the synchronizing circuit is configured to generate a signal to the read pointer responsive to the indication;

wherein said read pointer is configured to update to the pointer value from the first circuit responsive to the signal.

2. The circuit as recited in claim 1 wherein the pointer value is a write pointer value

of the write pointer concurrent with the indication, and wherein the circuit is a storage circuit configured to capture the write pointer value in response to the indication.

3. The circuit as recited in claim 1 further comprising a logic circuit coupled to the synchronizing circuit and configured to provide the indication.

4. The circuit as recited in claim 1, wherein the synchronizing circuit comprises a synchronizer for synchronizing the indication to the second clock signal.

5. The circuit as recited in claim 4, wherein the synchronizing circuit further comprises a delay circuit coupled to the synchronizer and configured to delay generation of the signal in response to the indication for a predetermined delay.

6. The circuit as recited in claim 5, wherein the delay circuit is clocked by the second clock.

7. The circuit as recited in claim 6, wherein the delay circuit comprises a predetermined number of flip-flops.

8. The circuit as recited in claim 6, wherein the delay circuit comprises a configurable number of flip-flops.

9. The circuit as recited in claim 1, wherein the write pointer includes a first counter which generates a write counter value, wherein the write counter value addresses the buffer.

10. The circuit as recited in claim 9, wherein the write counter is an up counter.

11. The circuit as recited in claim 1, wherein the read pointer includes a second

counter which generates a read counter value, wherein the read counter value addresses the buffer.

12. The circuit as recited in claim 11, wherein the read counter is an up counter.

13. The circuit as recited in claim 1, wherein the first circuit detects which of the plurality of entries in the buffer is updated with the predetermined pattern of data to generate the pointer value.

14. A method of initializing a buffer, the method comprising:

detecting a predetermined pattern of data transmitted for storage in one of a plurality of entries in the buffer responsive to a first clock;

generating a pointer value in response to the detecting;

synchronizing an indication of the detecting to a second clock;

updating a read pointer to said pointer value responsive to the synchronizing.

15. The method as recited in claim 14 wherein the synchronizing comprises delaying for a predetermined number of cycles of the second clock.

16. The method as recited in claim 14 further comprising generating a write pointer value used by a write pointer to indicate each one of said plurality of entries in the buffer.

17. The method as recited in claim 16, wherein the generating the write pointer value includes incrementing a first counter responsive to the second clock.

18. The method as recited in claim 14 further comprising generating a read pointer value used by the read pointer to indicate each one of said plurality of entries in the buffer.

19. The method as recited in claim 18, wherein said generating a read pointer value includes incrementing a second counter responsive to the second clock.

20. The method as recited in claim 14 wherein the generating a pointer value comprises capturing a write pointer value of the write pointer concurrent with the detecting.

21. The method as recited in claim 14 wherein the generating a pointer value comprises detecting which of the plurality of entries in the buffer is updated with the predetermined pattern of data.